



## SSC8029GN2

### P-Channel Enhancement Mode MOSFET

#### ➤ Features

VDS	VGS	RDS(on) Typ.	ID
-20V	±12V	18mR@-4V5	-7.5A
		21mR@-2V5	

#### ➤ Description

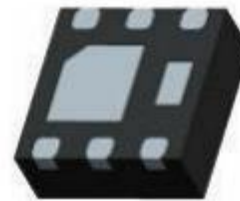
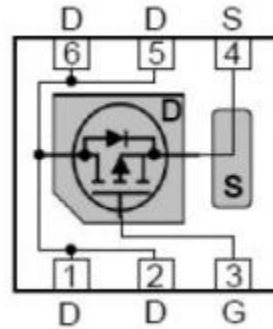
This device is produced with high cell density DMOS trench technology, uses advanced trench technology and design to provide excellent RDS(on) with low gate charge. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion
- Charging
- Driver for Relay

#### ➤ Pin configuration

Top view



Bottom View



Marking

#### ➤ Ordering Information

Device	Package	Shipping
SSC8029GN2	DFN2x2	3000/Reel



➤ **Absolute Maximum Ratings**( $T_A=25\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-7.5	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-24	A
$P_D$	Power Dissipation <sup>c</sup>	3	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	1.4	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction- to- Ambient Thermal Resistance <sup>a</sup>		99	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction- to- Case Thermal Resistance		45	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$  .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

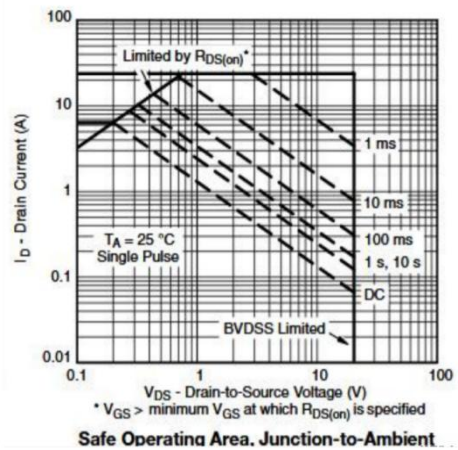
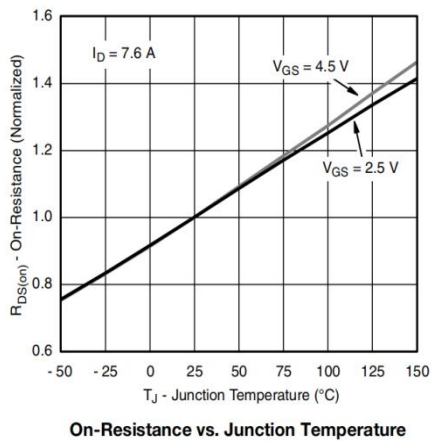
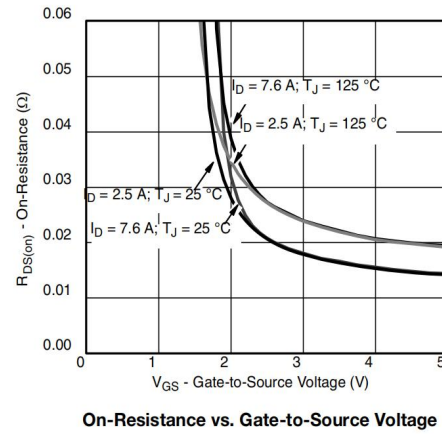
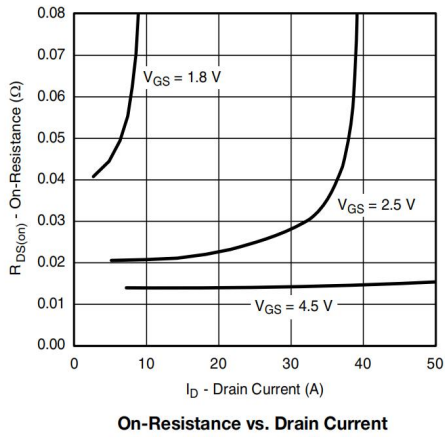
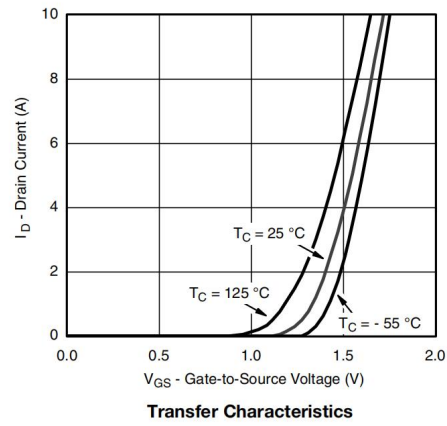
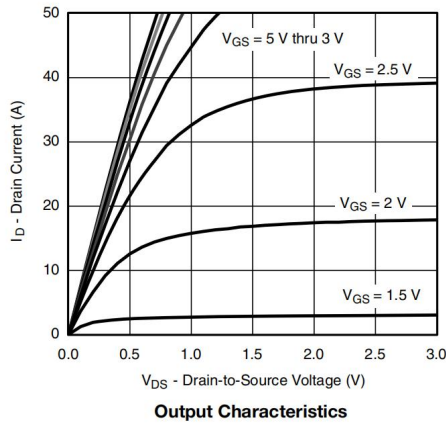


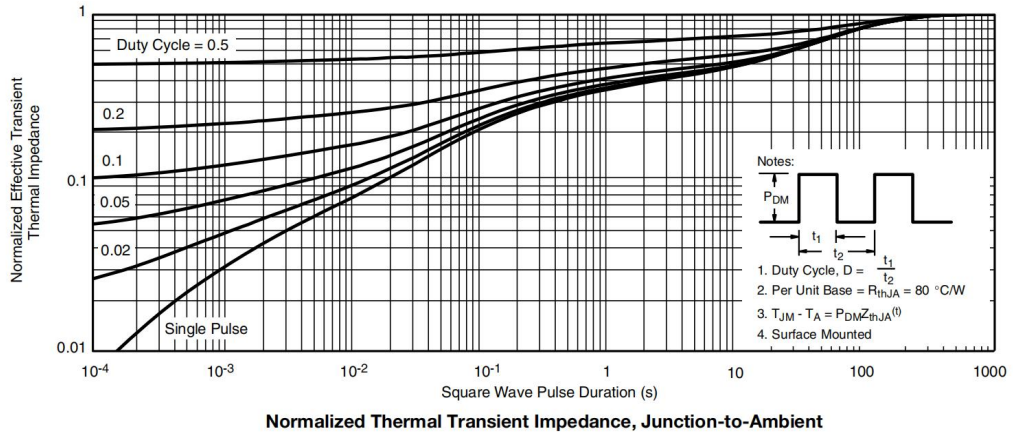
➤ **Electronics Characteristics**( $T_A=25^{\circ}C$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45	-0.55	-0.8	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-5.5A$		18	26	mR
		$V_{GS}=-2.5V, I_D=-2.5A$		21	30	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$			-1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=-5V, I_D=-5.5A$		23		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=-1A$		-0.75	-1.5	V
$C_{iss}$	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		1970		pF
$C_{oss}$	Output Capacitance			205		
$C_{rss}$	Reverse Transfer Capacitance			195		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-4.5V,$ $V_{DS}=-10V, R_L=6R,$ $R_G=6R, I_D=-6.5A$		16		ns
$T_r$	Rise time			14		
$T_{D(OFF)}$	Turn-off delay time			78		
$T_f$	Fall time			66		



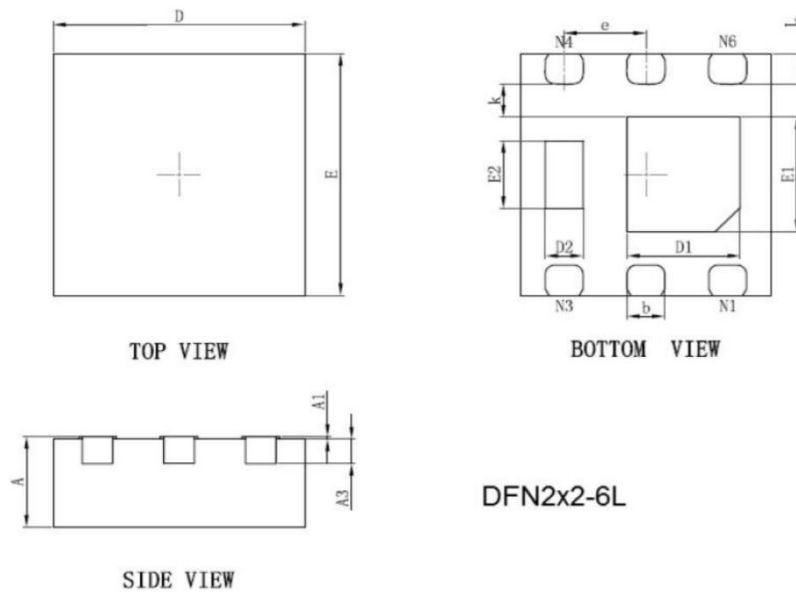
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)







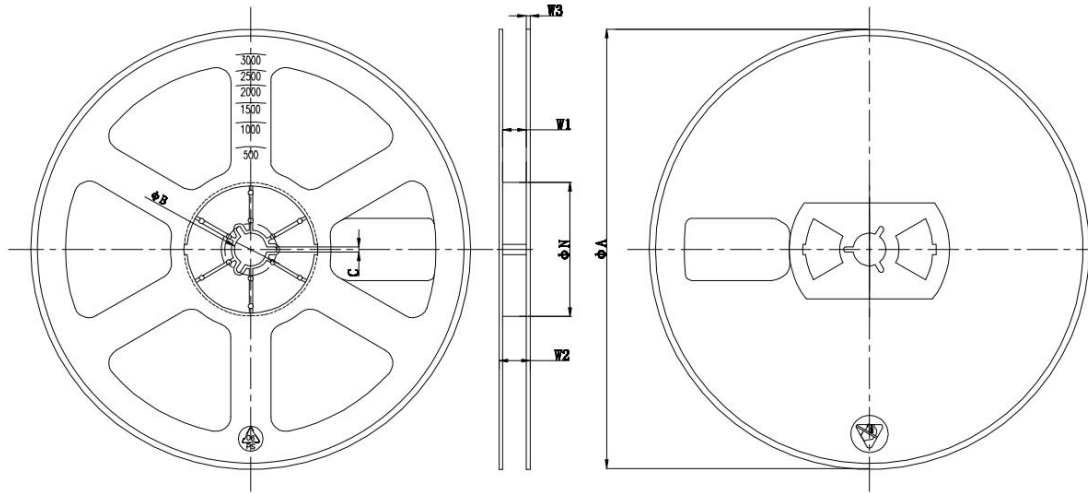
➤ Package Information



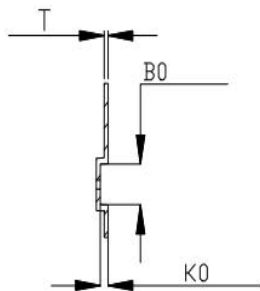
Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF.	
D	1.924	2.076
E	1.924	2.076
D1	0.800	1.000
E1	0.850	1.050
D2	0.200	0.400
E2	0.460	0.660
k	0.200MIN.	
b	0.250	0.350
e	0.650TYP.	
L	0.174	0.326



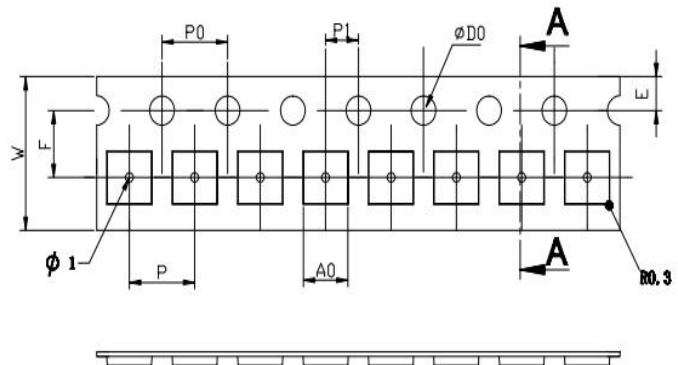
➤ Tape and Reel



$\phi A$	$\phi N$	$\phi B$	C	W1	W2	W3
178±2	54±2	13.2±0.3	2.2±0.3	9.5±1	13 <sub>max</sub>	1.4±0.4



剖面 A-A  
比例 4:1



A0	B0	K0	P	P0	E	F	D0	P1	T	W
2.25±0.05	2.25±0.05	1.15 ±0.05	4.00±0.05	4.00±0.05	1.75±0.10	3.50±0.05	1.55±0.10	2.00±0.05	0.25±0.05	7.95±0.05

说明:

1. 10个棘孔的累积误差不超过±0.2mm;
2. A0与B0的尺寸是距型腔内底部0.3mm处测得;
3. K0的尺寸是型腔内底部到料带上表面的距离;
4. 料带厚度0.25±0.5mm;
5. 材料: 黑色PS.



➤ **Revision History**

V1.0	Product Datasheet	
V2.2	Add Tape and Reel	2022.8.30

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